The PROFIBUS DP Slave IP Core and the protocol software executed inside the FPGA comprise all digital functions required for implementing a PROFIBUS DP slave. The product thus eliminates the need for a specific additional fieldbus controller ASIC.

**Minimum Development Effort**
- Combination of all components required for implementing a PROFIBUS DP Slave on a Field Programmable Gate Array (FPGA)
- PROFIBUS DP bus control logic implemented as loadable IP Core
- PROFIBUS DP protocol stack ready-to-use on soft core processor within FPGA
- Including PROFIBUS versions DP (exchange of cyclic data and diagnosis) and DP-V1 (acyclic data exchange and extended diagnosis)

**One API For Quick Integration**
- Simple Device Application Interface (SDAI) designed as efficient protocol abstraction layer to use different protocols with same application
- PROFIBUS, PROFINET IRT, EtherCAT, EtherNet/IP, POWERLINK and Modbus TCP using the same API
- Device application software running on second processor inside the FPGA or on separate external host processor

**Space-Saving and Future-Proof Implementation**
- Provision of complete bus control logic for accessing PROFIBUS DP network
- Handling of all time-critical parts of PROFIBUS DP Data Link Layer and cyclic data exchange
- No dependency on fieldbus controller ASIC and its vendor

**Flexible, Scalable and Low-Maintenance Solution**
- Possibility to use different protocols alternatively or in parallel, also with multiple channels
- Easily extensible by customer-specific functions thanks to FPGA technology
- Easy integration of future versions
- Same license model for all protocols
## Technical Data

### Hardware
- **Qsys Subsystem**
  - IP Core with PROFIBUS DP bus control logic
  - 1 Nios II IP Core for protocol processing
  - DPRAM (4 KB) interface to application
  - Memory-mapped bridges for Flash and RAM

- **PROFIBUS Clocks**
  - Nios II Clock
  - Configurable (default: 75 MHz)

### Software
- **PROFIBUS Functionality**
  - PROFIBUS DP Slave
  - PROFIBUS DP, PROFIBUS DP-V1
  - Cyclic services
  - Sync / Freeze
  - Input / output data: up to 244 Bytes each
  - Configuration / parameter / diagnosis data: up to 244 Bytes each
  - Acyclic Read / Write (Master Class 1 and Class 2)
  - Up to 3 simultaneous Master Class 2 connections
  - Automatic baud rate recognition
  - Identification & Maintenance services (IM0)
  - Modular slave with up to 64 modules
  - Support of dynamic I/O configuration change by Slave application
  - Diagnostic alarms and Pull/Plug alarms
  - Support of redundancy switch over command

### Conformity
- Tested with PROFIBUS DP Tester Software

### System Requirements
- **FPGA Type**
  - Altera Cyclone IV or V (and SoC)
- **FPGA Resources**
  - Approximately 5,000 ALMs, 32 M10k memory blocks
- **Memory**
  - Code and initialized data: approximately 470 KB

### Licensing
- Per Unit Base or Annual Base

## Scope of Delivery

### IP Core
- PROFIBUS DP Slave IP, Qsys subsystem for PROFIBUS Slave
- Sample FPGA design

### Software
- PROFIBUS DP Slave stack, binary format
- Sample application for “Evaluation Kit Altera Cyclone V E”
- Sample device description file (GSD)
- Sample projects for Siemens PLCs and Softing configurator

### Documentation
- PROFIBUS Slave user manual, SDAI manual (electronic format)

## Order Numbers
- **ISL-YY-015320**
  - Per Unit License for One Slave Device (security EEPROM, packing unit: 250 pieces)
- **LAA-NN-019320**
  - Annual Product License Fee (right to sell an unlimited number of a single customer product for one year)

## Additional Products and Services
- **SIA-NN-018101**
  - PROFIBUS DP Integration Workshop
- **TRA-PB-TECH**
  - PROFIBUS Technology Training
- **DDA-NN-006014**
  - PROFIBUS Tester 5 (BC-700-PB)