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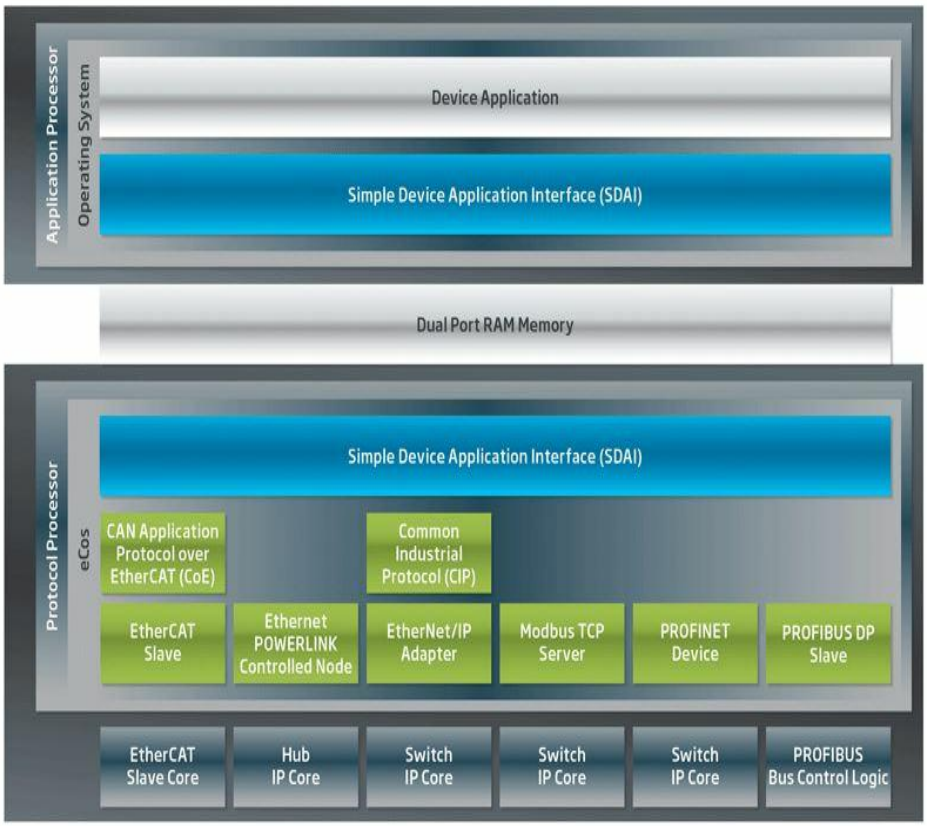
**Licensing Guide**

# Protocol IP License Authentication





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## Disclaimer of liability

The information contained in these instructions corresponds to the technical status at the time of printing of it and is passed on with the best of our knowledge. The information in these instructions is in no event a basis for warranty claims or contractual agreements concerning the described products, and may especially not be deemed as warranty concerning the quality and durability pursuant to Sec. 443 German Civil Code. We reserve the right to make any alterations or improvements to these instructions without prior notice. The actual design of products may deviate from the information contained in the instructions if technical alterations and product improvements so require.



**Softing Industrial Automation GmbH**

Richard-Reitzner-Allee 6
85540 Haar / Germany
http://industrial.softing.com
+ 49 89 4 56 56-0
+ 49 89 4 56 56-488
info.automation@softing.com
support.automation@softing.com

The latest version of this manual is available in the Softing download area at: http://industrial.softing.com/en/downloads.html

# Table of Contents

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# 1 About this document

*Softing Protocol IP* is a proprietary term describing the Softing intellectual property (IP) that is used to implement Industrial Ethernet and Profibus devices on Intel FPGAs. It consists of loadable logic (IP cores), protocol stack software, sample designs and documentation.

This document describes how Softing Protocol IP solutions are licensed for Industrial Ethernet including the protocols EtherCAT, EtherNet/IP, MODBUS TCP, Ethernet POWERLINK and PROFINET.

For downloading the most recent solution visit the Softing Download center Softing download page (http://industrial.softing.com/en/downloads.html).

For most recent licensing updates please visit https://www.altera.com/solutions/industry/industrial/applications/automation/industrial-networking.html#production.

# 2 License authentication

Softing uses an authentication interface to prevent unauthorized use of IP blocks. For this purpose, an external security chip (pre-programmed MAXII) is connected to the interface. The IP block sends authentication requests cyclically to the connected security chip and verifies the responses. The security chip response with a notification telling the IP block that it uses a valid license.

The authentication interface is purposely slow to provide maximum flexibility in routing paths on the chip and board. For example, data is driven out on the rising edge of the clk_shift and sampled on the negative edge of the clk_shift, which allows for maximum setup/hold conditions. clk_shift is treated as a data signal, not as a true "clock" internally to the CPLD, so there is no need for additional board constraints that would normally be afforded to a clock signal.

Without a valid license, the IP core still works for the period specified below, making it possible for customers to evaluate the IP core. If this period is expired, the customer can power cycle the system again and make use of a succeeding evaluation period.

| Protocol | Evaluation period |
|---|---|
| EtherCAT with ESC30 | 15 minutes |
| PROFINET, EtherNet/IP, MODBUS TCP, Ethernet POWERLINK | 2 hours |

The following table lists the corresponding Intel part numbers for various protocols:

| Protocol | Intel® Part Number |
|---|---|
| All protocols (except EtherCAT with ESC30) | M570ZM6NKA |
| All protocols (except EtherCAT with ESC30) | M570F11NBA |
| All protocols (including EtherCAT with ESC30) | M570ZM6NLA |
| All protocols (including EtherCAT with ESC30) | M570F11NCA |

Security chips can be purchased from Intel® and from authorized Intel distributors. For further information visit the Intel contact page.

# 3 Signals

This section describes the connection between IP Core and CPLD and what needs to be considered when integrating the CPLD into the final hardware.

The rst_System_n of the CPLD can be connected and controlled by the FPGA. If so, it is necessary to have an additional connection between CPLD and FPGA. Connecting this signal to the FPGA reset is a second solution. In this case the CPLD always starts after power up and cannot be controlled by any logic in the FPGA.

All unused IO pins of the CPLD must be left open, i.e. must not be connected.

**Note**
For a full and detailed signal plan of the CPLD please contact Intel® or your local distributor.

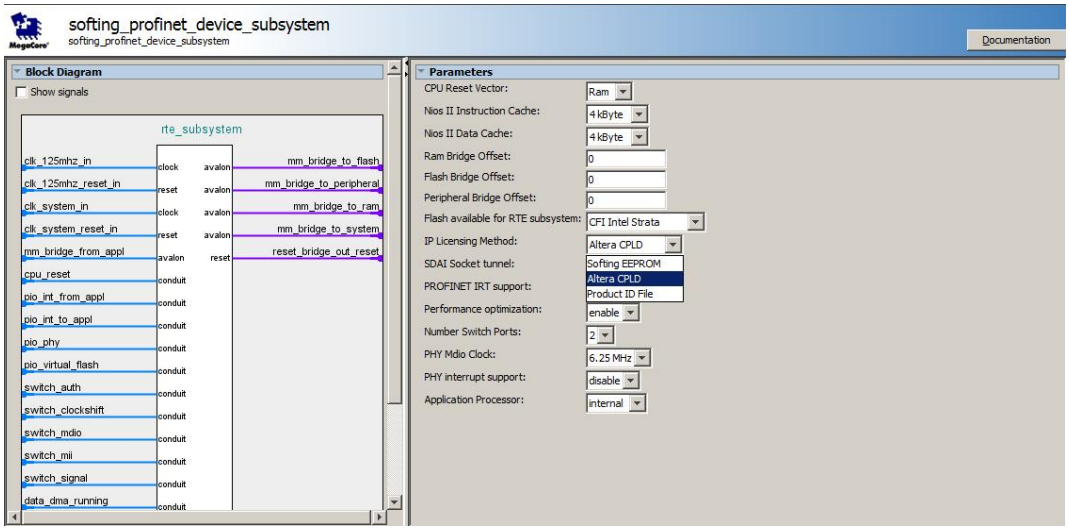
| **FPGA** | | **CPLD EPM570M100 Pkg/Ordering code M570ZM6NKA or M570ZM6NLA** | | |
|---|---|---|---|---|
| Signal_Name | Direction | Signal_Name | Direction | PIN |
| PortOutClk | Output | Clk_shift | Input | E1 |
| PortOutDataValid | Output | Chal_valid | Input | E11 |
| PortOutData | Output | Chal_data | Input | C11 |
| PortInDataInValid | Input | Resp_valid | Output | J11 |
| PortInDataIn | Input | Resp_data | Output | C1 |
| | | Rst_System_n | Input | G11 |

| **FPGA** | | **CPLD EPM570F100 Pkg/Ordering code M570F11NCA or M570F11NBA** | | |
|---|---|---|---|---|
| Signal_Name | Direction | Signal_Name | Direction | PIN |
| PortOutClk | Output | Clk_shift | Input | E1 |
| PortOutDataValid | Output | Chal_valid | Input | C10 |
| PortOutData | Output | Chal_data | Input | A10 |
| PortInDataInValid | Input | Resp_valid | Output | G10 |
| PortInDataIn | Input | Resp_data | Output | C1 |
| | | Rst_System_n | Input | E10 |

## 3.1 MAX II devices

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple VCC levels on the VCCINT supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device. (more details can be found in MAX II Device Handbook https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/max2/max2_mii5v1.pdf )

Selection regarding use of CPLD has to be made in the QSys component. The picture below shows the configuration interface of the PROFINET QSys component. There are comparable configuration interfaces for the other protocol subsystems available.




Please check the appropriate *Softing Protocol IP* subsystem documentation (Quick Startup Guide, available together with the IP Protocol software from our Download Center at http://industrial.softing.com/en/downloads.html) and set the license type parameters in the QSys top level design.

You will find further documentation in the protocol-specific subdirectory ..\hardware\documentation of the unzipped downloaded file.

# 4 Glossary

| Acronym | Meaning |
|---|---|
| CPLD | Complex Programmable Logic Device |
| FPGA | Field Programmable Gate Array |
| IP | Intellectual Property |
| LVTTL | Low Voltage Transistor-Transistor Logic |

**Softing Industrial Automation GmbH**

Richard-Reitzner-Allee 6
85540 Haar / Germany
http://industrial.softing.com

Tel: + 49 89 45 656-0
Fax: + 49 89 45 656-488
info.automation@softing.com