PROFIBUS DP Master for Xilinx FPGA

Full Set of Protocol Stack and Fieldbus Controller Functionality Ready-to-Use for FPGA

The PROFIBUS DP Master for Xilinx FPGA integrates components required for implementing a complete PROFIBUS DP Class 1 and Class 2 Master based on FPGA technology. Thus, no specific fieldbus controller ASIC is needed in addition.

Minimum Development Effort

- Combination of all components required for implementing a PROFIBUS DP Class 1 or Class 2 Master into a Field Programmable Gate Array (FPGA)
- PROFIBUS DP bus control logic available as loadable IP Core
- PROFIBUS DP protocol stack ready to be used on soft core processor within FPGA
- Control application running on second processor inside the FPGA or on separate external host processor
- Including PROFIBUS DP versions DP (exchange of cyclic data and diagnosis with slaves), DP-V1 (acyclic data exchange and alarm handling) as well as DP-V2 (clock synchronization and time-stamping)

Flexibility Through Integrated Fieldbus Controller

- Provision of complete bus control logic for accessing PROFIBUS DP network
- Handling of all time-critical parts of PROFIBUS DP Data Link Layer, token handling and cyclic data exchange
- No dependency on fieldbus controller ASIC and its vendor

Improved Plant Availability

- Support of Master redundancy providing seamless switchover from primary to backup PROFIBUS DP Master
- Optional line redundancy functionality for accessing field devices via redundant fieldbus cables
- Support of re-configuring individual PROFIBUS slaves without shutting-down plant
Technical Data

Supported Slave Devices ≤ 125
Total Cyclic Input / Output Data ≤ 30,500 Bytes / ≤ 30,500 Bytes
Input / Output Data Per Slave ≤ 244 Bytes / ≤ 244 Bytes
Configuration / Parameter / Diagnostic Data Per Slave ≤ 244 Bytes / ≤ 244 Bytes / ≤ 244 Bytes

Protocols PROFIBUS DP-V0, PROFIBUS DP-V1, PROFIBUS DP-V2

PROFIBUS DP-V1 Features
- Alarms
- Extended Diagnostics
- Acyclic Read/Write (Class 1 and Class 2)
- Data Transfer (Load Region)

Additional Features
- Online Change (re-configuration of individual slaves while the rest of the plant continues operating)
- Diagnostic History (storage of diagnostic messages in a FIFO of configurable size until they are read by the application)
- Optional synchronization between PROFIBUS DP poll cycle and application
- Preprocessing of input data (the application is notified when data have changed)

Optional Features (Part of Pro Version)
- Master Redundancy (Seamless Master Switchover, Requires Redundancy Link Between Active Master and Backup Master)
- PROFIBUS DP-V2 Features (Clock Synchronization, Time Stamps)

Optional Feature (Separate Item)
Line Redundancy (operates two independent physical connections)

System Requirements
- Memory Code: 512 KB, RAM: 512 KB
- FPGA Xilinx Zynq, 7 Series, Spartan 6
- FPGA resources for typical design comprising PROFIBUS subsystem (IP Core and protocol stack on MicroBlaze) and application subsystem (running on second MicroBlaze)
- LUTs 16 K (approximately 25 K Logic Cells)
- Block RAM Tiles 32 (for maximum system), can be downscaled

Licensing Per Unit Base or Annual Base

Scope of Delivery

IP Core PROFIBUS DP bus control logic, sample FPGA design for ZedBoard (utilizing Zynq-7000 AP SoC XC7Z020)

Software
- PROFIBUS DP Master stack, binary format
- PROFIBUS Access Kit (allows porting of the protocol access library regarding hardware, operating system and application software), source format
- PROFIBUS Sample Application (precompiled for instant use with second soft core processor of sample design), source format

Documentation „PROFIBUS DP Stack” manual and „PROFIBUS Master for Xilinx FPGA” user manual, electronic format

Order Numbers

PROFIBUS DP Master, IP Core and Protocol Stack (DP-V0, DP-V1, Without Master Redundancy)
- KXL-NN-016413 Development Package (includes software and documentation, required for both license models)
- ISL-YY-015310 Per Unit License for One Master Device (security EEPROM, packing unit: 250 pieces)
- LAA-NN-019310 Annual Product License Fee (right to sell an unlimited number of a single customer product for one year)
- LFA-NN-019340 Option PROFIBUS DP Line Redundancy for PROFIBUS DP Master IP Core (one-time fee for one customer product)

PROFIBUS DP Master pro, IP Core and Protocol Stack (DP-V0, DP-V1, DP-V2 and Master Redundancy)
- KXL-NN-016413 Development Package (includes software and documentation, required for both license models)
- ISL-YY-015311 Per Unit License for One Master Device (security EEPROM, packing unit: 250 pieces)
- LAA-NN-019311 Annual Product License Fee (right to sell an unlimited number of a single customer product for one year)
- LFA-NN-019340 Option PROFIBUS DP Line Redundancy for PROFIBUS DP Master IP Core (one-time fee for one customer product)

Additional Products and Services

IAPB Integration Project
SIA-NN-018101 PROFIBUS DP Integration Workshop
DDA-NN-006014 PROFIBUS Tester 5 (BC-700-PB)
TRA-PB-TECH PROFIBUS Technology Training