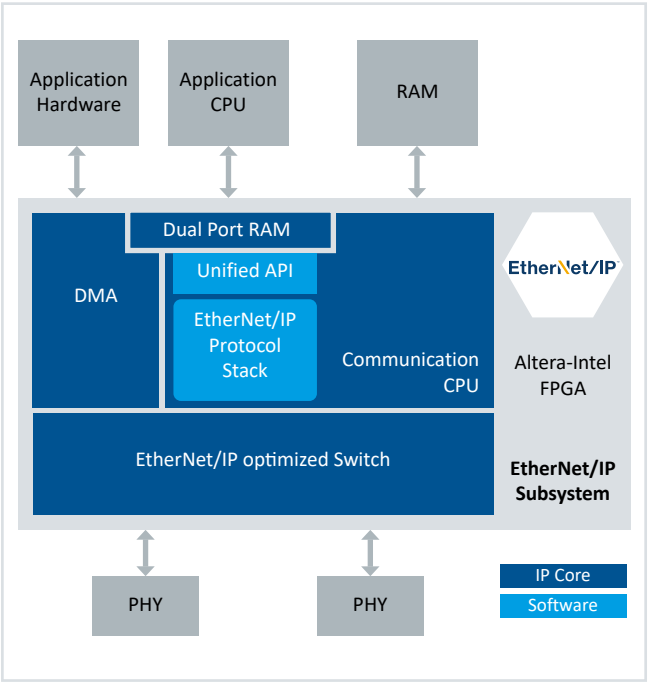
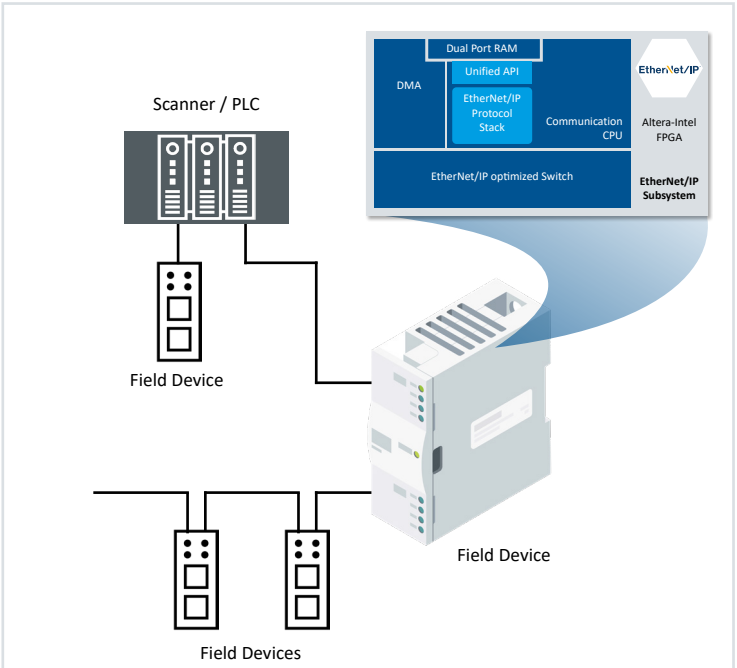
EtherNet/IP Adapter Subsystem for Altera-Intel FPGA

Switch IP Core and Communication Processor for the Integration of EtherNet/IP on Altera-Intel FPGA

- **Simplifies EtherNet/IP connectivity for field devices with Altera-Intel FPGA**
- **Optimized switch IP core and pre-installed software handle the entire protocol**
- **EtherNet/IP and other industrial networks are supported by the same API**
- **Fast and robust operation by hardware/logic support and redundancy features**





Easy-to-Integrate EtherNet/IP Adapter Subsystem for FPGAs

- Entire protocol is handled by pre-installed software, no need for any porting
- Example project for fast hands-on experience
- Adaptation to the application requirements by extensive configuration options
- Large choice of supported FPGA families and sizes

Low Total Cost of Ownership

- No dependency on special ASICs
- Risk-free implementation thanks to Softing's consulting, integration, and pre-certification services
- Re-configuration and extension possible even after production
- Simple addition of further protocols

Pre-certified to Latest Standards

- Compliant to current EtherNet/IP specifications
- Can act as "black channel" for safety applications
- Media redundancy supported (DLR)

Fast and Robust Operation

- Industrial switch IP core with cut-through forwarding and filtering (firewall)
- Data handling in software or hardware (DMA)
- Device application software is separated from protocol software
- Cycle times down to 100 µs

EtherNet/IP Adapter Subsystem for Altera-Intel FPGA

Technical Data

IP Core configuration	▪ Switch IP core with 2 external ports and 1 or 2 internal ports ▪ Communication CPU IP core for processing the EtherNet/IP protocol ▪ DPRAM interface to application processor (FPGA-internal or external)
Switch clock	125 MHz
Supported FPGA families	Cyclone III, Cyclone IV, Cyclone V, Cyclone V SoC, Cyclone 10 LP, MAX 10
Functionality	▪ EtherNet/IP Adapter compliant to ODVA conformance test CT-20 ▪ Media Redundancy (Device Level Ring; announce-based and beacon-based) ▪ LLDP protocol ▪ Quality of Service (QoS) supported ▪ Support for Quick Connect ▪ Communication support for CIP Safety ▪ Optional 2nd internal switch port for direct connection of the application CPU ▪ Optional hardware acceleration (DMA)
Cycle time	down to 100 µs
Number of connections	▪ Support for up to 10 concurrent I/O Connections ▪ Support for up to 10 concurrent Encapsulation Sessions ▪ Support for at least 2 concurrent Explicit Messaging Connections (minimum guaranteed number) for each Encapsulation Session ▪ Support for up to 6 additional Explicit Messaging Connections to be used by any client
Application Programming Interface	Simple Device Application Interface (SDAI)

Scope of Delivery

IP / Logic	▪ Complete EtherNet/IP Adapter subsystem ▪ Supplementary IP cores ▪ Sample application FPGA design
Software	▪ Ready-to-run protocol software (executable) for the EtherNet/IP Adapter subsystem ▪ API library for the application processor (including source code) ▪ Sample application software (including source code)
Documentation	Download: EtherNet/IP subsystem implementation guide and additional information

Order Numbers

Please contact us for details	**EtherNet/IP Adapter Subsystem for Altera-Intel FPGA** We are happy to discuss your particular requirements and adequate licensing options with you.

Additional Products and Services

SIA-YY-012501	Integration workshop for implementing EtherNet/IP
SIA-YY-012503	Integration support provided by e-mail or phone
Please contact us for details	Integration and pre-certification services

Your local Softing contact:

https://industrial.softing.com

optimize! softing

Technical changes reserved © Softing Industrial Automation GmbH, EtherNet-IP_Subsystem_Altera-Intel_FPGA_D_EN_240411_100, April 2024