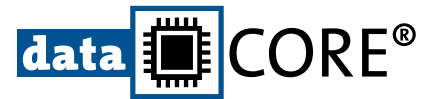
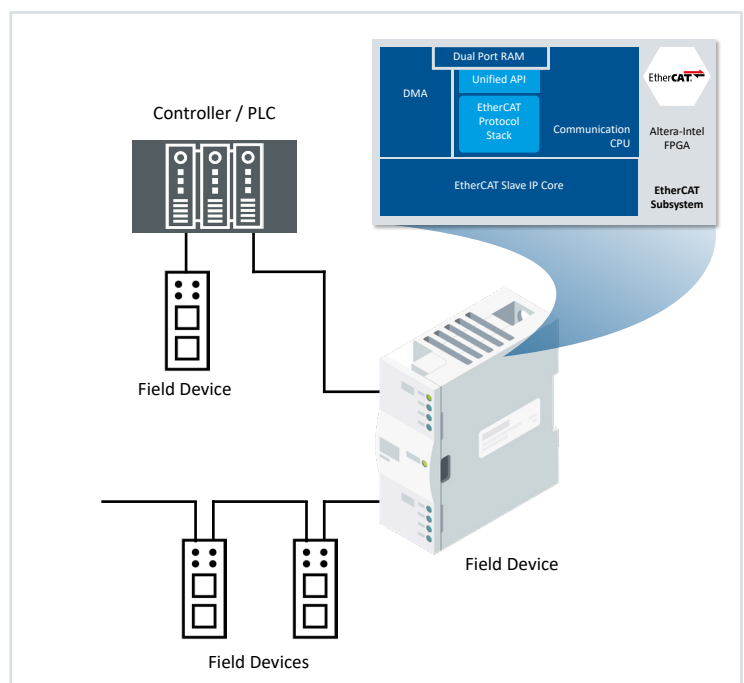
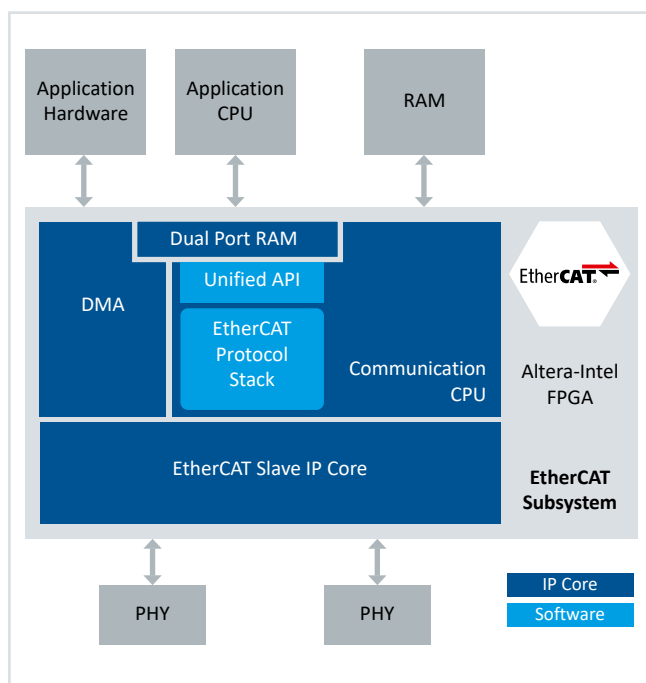


EtherCAT Subsystem for Altera-Intel FPGA



EtherCAT Slave IP Core and Communication Processor for the Integration of EtherCAT on Altera-Intel FPGA

- Simplifies EtherCAT connectivity for field devices with Altera-Intel FPGA
- Optimized EtherCAT IP core and pre-installed software handle the entire protocol
- EtherCAT and other industrial networks are supported by the same API
- Fast and robust operation by hardware/logic support and redundancy



Easy-to-Integrate EtherCAT Slave Subsystem for FPGAs

- Entire protocol is handled by pre-installed software, no need for any porting
- Example project for fast hands-on experience
- Adaptation to the application requirements by extensive configuration options
- Large choice of supported FPGA families and sizes

Low Total Cost of Ownership

- No dependency on special ASICs
- Risk-free implementation thanks to Softing's consulting, integration, and pre-certification services
- Re-configuration and extension possible even after production
- Simple addition of further protocols

Pre-certified to Latest Standards

- Compliant to current EtherCAT specifications
- Tested with conformance test V2.5.0.0

Fast and Robust Operation

- EtherCAT Slave IP core with cut-through forwarding and media redundancy
- Data handling in software or hardware (DMA)
- Device application software is separated from protocol software
- Cycle times down to 50 μ s

EtherCAT Subsystem for Altera-Intel FPGA

Technical Data

IP Core configuration	<ul style="list-style-type: none">▪ EtherCAT Slave with two Ethernet ports▪ Communication CPU IP core for processing the EtherCAT protocol▪ DPRAM interface to application processor (FPGA-internal or external)
Supported FPGA families	Cyclone III, Cyclone IV, Cyclone V, Cyclone V SoC, Cyclone 10 LP, MAX 10
Functionality	<ul style="list-style-type: none">▪ EtherCAT Slave Device compliant to ETG conformance test V2.5.0.0▪ 4 Sync Managers▪ 3 FMMUs▪ EtherCAT state machine supported▪ Distributed Clocks supported▪ Generation of synchronous output signals (SYNC0/1)▪ Ethernet over EtherCAT (EoE) supported, used for devices with TCP/IP stack▪ CANopen over EtherCAT (CoE) for acyclic communication▪ File access over EtherCAT (FoE) to upload/download file▪ Object dictionary with standard CoE objects already implemented▪ Integration of application objects possible via SDAI▪ SDO Upload/Download and SDO information services supported▪ Support for multiple PDOs (customizable)▪ PDI and Process Data watchdog supported▪ Writable PDO Mapping and Assignment Objects▪ EtherCAT Emergencies, Error Register and Diagnosis history object▪ Station Alias and ID Selector▪ Optional hardware acceleration (DMA)
Cycle time	down to 50 μ s
Application Programming Interface	Simple Device Application Interface (SDAI)

Scope of Delivery

IP / Logic	<ul style="list-style-type: none">▪ Complete EtherCAT slave subsystem▪ Supplementary IP cores▪ Sample application FPGA design
Software	<ul style="list-style-type: none">▪ Ready-to-run protocol software (executable) for the EtherCAT slave subsystem▪ API library for the application processor (including source code)▪ Sample application software (including source code)
Documentation	Download: EtherCAT subsystem implementation guide and additional information

Order Numbers

[Please contact us for details](#)

EtherCAT Slave Subsystem for Altera-Intel FPGA

We are happy to discuss your particular requirements and adequate licensing options with you.

Additional Products and Services

SIA-YY-012501	Integration workshop for implementing EtherCAT
SIA-YY-012503	Integration support provided by e-mail or phone
Please contact us for details	Integration and pre-certification services

Your local Softing contact:

<https://industrial.softing.com>

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